WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a layer of insulation material formed over a semiconductor substrate; and

a metal trace formed in the layer of insulation material, the metal trace having a base region and a plurality of spaced-apart fingers that extend away from the base region.

2. The semiconductor device of claim 1 wherein the metal trace forms a number of loops.

3. The semiconductor device of claim 2 wherein the loops lie substantially in a same plane.

4. The semiconductor device of claim 1 wherein the metal trace has a first end and a second end.

5. The semiconductor device of claim 4 wherein the second end is connected to a via.

6. The semiconductor device of claim 1 wherein the fingers extend away from a bottom surface of the base region.

7. A method of forming a semiconductor device, the method comprising the steps of:

forming a layer of insulation material over a semiconductor substrate, the layer of insulation material having a first opening that defines a first side wall and an opposing second side wall;

forming a first layer of conductive material on the layer of insulation material to fill up the first opening;

anisotropically etching the first layer of conductive material to form a first conductive spacer that adjoins the first side wall and the second side wall, and a second opening;

forming a first layer of isolation material on the layer of insulation material and the first conductive spacer to fill up the second opening; and

forming a conductive region on the first conductive spacer and the first layer of isolation material, the conductive region making an electrical connection with the first conductive spacer.

8. The method of claim 7 and further comprising the steps of:

anisotropically etching the first layer of isolation material to form a first isolation spacer that adjoins the first conductive spacer, and a third opening;

forming a second layer of conductive material on the layer of insulation material to fill up the third opening;

anisotropically etching the second layer of conductive material to form a second conductive spacer that adjoins the first isolation spacer, and a fourth opening;

forming a second layer of isolation material on the layer of insulation material and the first conductive spacer to fill up the fourth opening,

the conductive region making an electrical connection with the first and second conductive spacers.

9. The method of claim 7 and further comprising the step of planarizing the layer of insulation material, the first conductive spacer, and the first layer of isolation material until the layer of insulation

material, the first conductive spacer, and the first layer of isolation material have a substantially planar top surface.

10. The method of claim 8 and further comprising the step of planarizing the layer of insulation material, the first conductive spacer, and the first layer of isolation material until the layer of insulation material, the first conductive spacer, and the first layer of isolation material have a substantially planar top surface.

11. The method of claim 7 wherein the step of forming a conductive region includes the steps of:

forming a second layer of conductive material on the layer of insulation material, the first conductive spacer, and the first layer of isolation material;

forming a mask on the second layer of conductive material that exposes regions of the second layer of conductive material; and

etching the exposed regions of the second layer of conductive material.

12. The method of claim 8 wherein the step of forming a conductive region includes the steps of:

forming a third layer of conductive material on the layer of insulation material, the first conductive spacer, the first layer of isolation material, and the second conductive spacer;

forming a mask on the third layer of conductive material that exposes regions of the third layer of conductive material; and

etching the exposed regions of the third layer of conductive material.

13. The method of claim 7 wherein the first opening is formed to have a number of loops.

14. The semiconductor device of claim 13 wherein the loops lie substantially in a same plane.

15. The method of claim 14 wherein the first opening exposes a via.